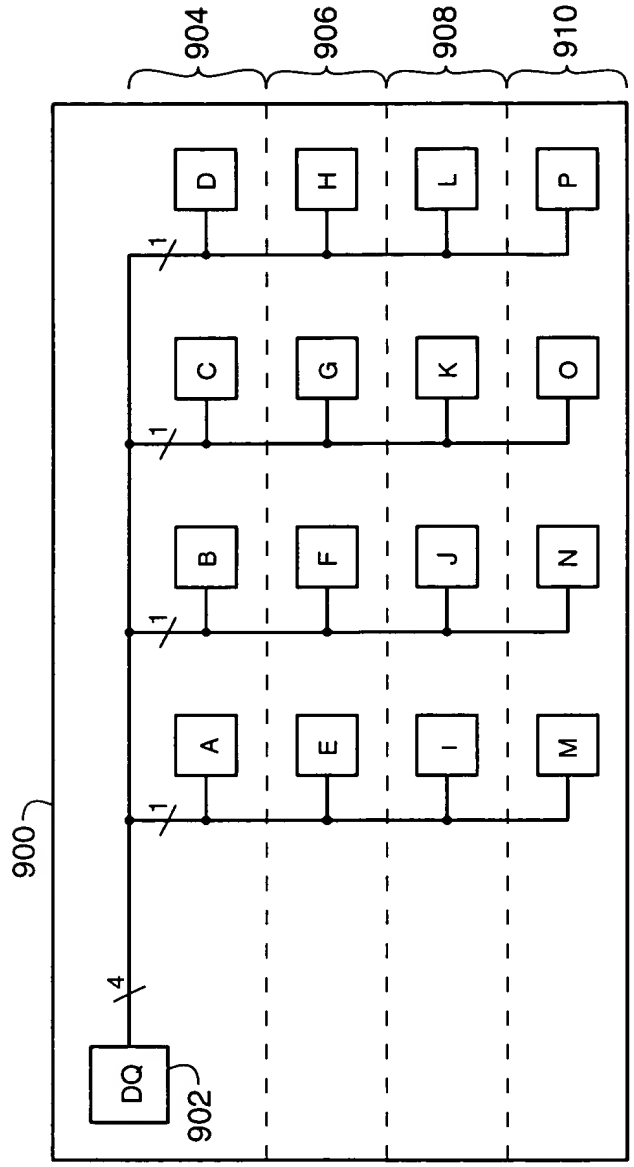

FIG. 1
(PRIOR ART)

	CLOCK CYCLE PRIOR ART TEST METHOD	CLOCK CYCLE EXEMPLARY TEST METHOD
1	WRITE TO 1ST ADDR OF CHIPS A, B, C, & D	WRITE TO 1ST ADDR OF CHIPS A, B, C, & D
2	WRITE TO 2ND ADDR OF CHIPS A, B, C, & D	WRITE TO 2ND ADDR OF CHIPS A, B, C, & D
3	WRITE TO 3RD ADDR OF CHIPS A, B, C, & D	WRITE TO 3RD ADDR OF CHIPS A, B, C, & D
4	WRITE TO 4TH ADDR OF CHIPS A, B, C, & D	WRITE TO 4TH ADDR OF CHIPS A, B, C, & D
5	READ FROM 1ST ADDR OF CHIP A	READ FROM 1ST ADDR OF CHIPS A, B, C, & D
6	READ FROM 2ND ADDR OF CHIP A	READ FROM 2ND ADDR OF CHIPS A, B, C, & D
7	READ FROM 3ND ADDR OF CHIP A	READ FROM 3RD ADDR OF CHIPS A, B, C, & D
8	READ FROM 4TH ADDR OF CHIP A	READ FROM 4TH ADDR OF CHIPS A, B, C, & D
9	READ FROM 1ST ADDR OF CHIP B	READ FAIL FLAG FROM A
10	READ FROM 2ND ADDR OF CHIP B	READ FAIL FLAG FROM B
11	READ FROM 3RD ADDR OF CHIP B	READ FAIL FLAG FROM C
12	READ FROM 4TH ADDR OF CHIP B	READ FAIL FLAG FROM D
13	READ FROM 1ST ADDR OF CHIP C	
14	READ FROM 2ND ADDR OF CHIP C	
15	READ FROM 3RD ADDR OF CHIP C	
16	READ FROM 4TH ADDR OF CHIP C	
17	READ FROM 1ST ADDR OF CHIP D	
18	READ FROM 2ND ADDR OF CHIP D	
19	READ FROM 3RD ADDR OF CHIP D	
20	READ FROM 4TH ADDR OF CHIP D	

FIG. 2

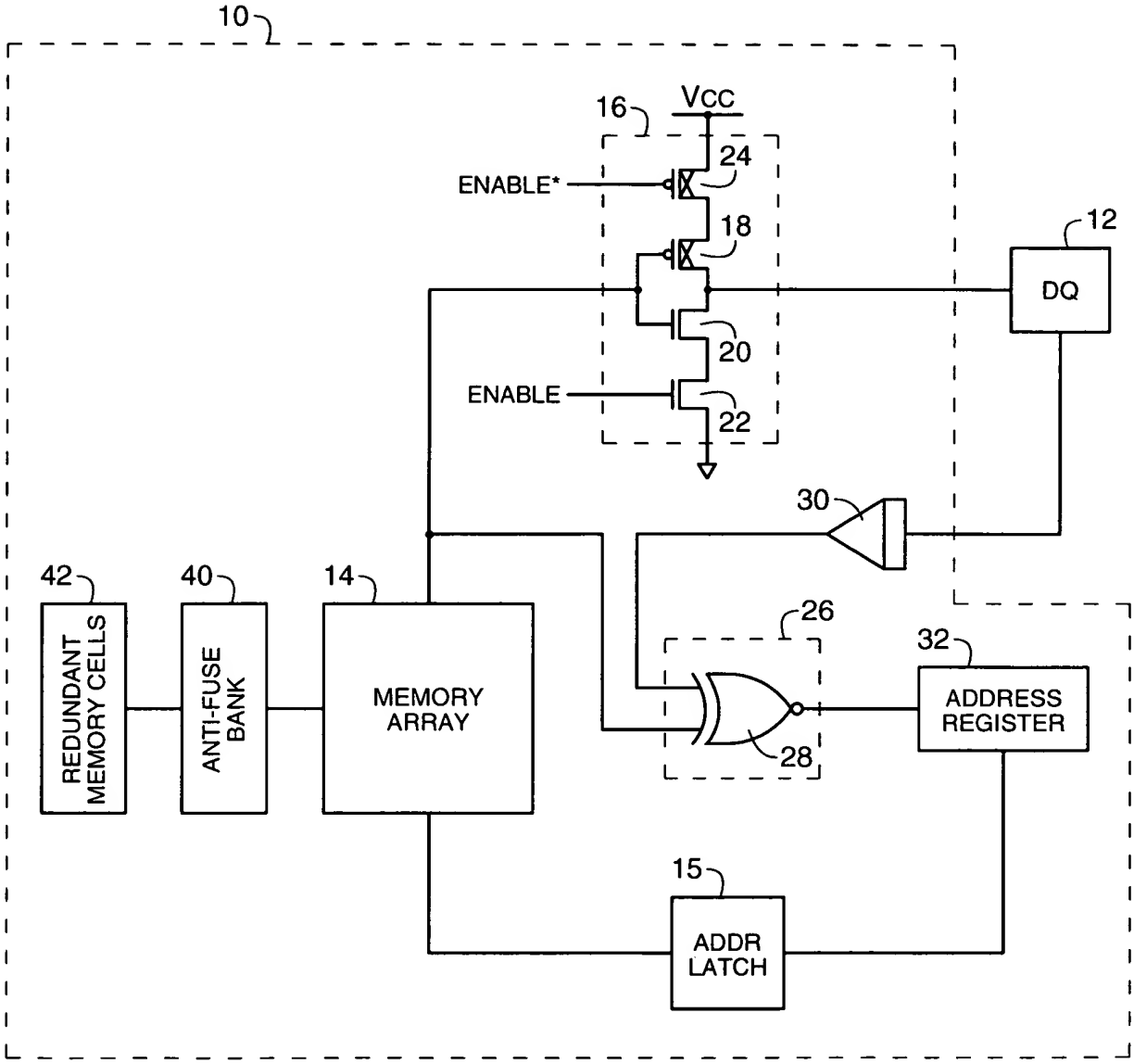
10
16
Vcc
24
ENABLE*
18
12
DQ
20
ENABLE
22
30
42
40
14
26
32
REDUNDANT MEMORY CELLS
ANTI-FUSE BANK
MEMORY ARRAY
ADDRESS REGISTER
28
15
ADDR LATCH

FIG. 3

	CLOCK CYCLE PRIOR ART TEST METHOD	CLOCK CYCLE EXEMPLARY TEST METHOD
1	WRITE TO 1ST ADDR OF CHIPS A, B, C, & D	WRITE TO 1ST ADDR OF CHIPS A, B, C, & D
2	WRITE TO 2ND ADDR OF CHIPS A, B, C, & D	WRITE TO 2ND ADDR OF CHIPS A, B, C, & D
3	WRITE TO 3RD ADDR OF CHIPS A, B, C, & D	WRITE TO 3RD ADDR OF CHIPS A, B, C, & D
4	WRITE TO 4TH ADDR OF CHIPS A, B, C, & D	WRITE TO 4TH ADDR OF CHIPS A, B, C, & D
5	WRITE TO 5TH ADDR OF CHIPS A, B, C, & D	WRITE TO 5TH ADDR OF CHIPS A, B, C, & D
6	READ FROM 1ST ADDR OF CHIP A	READ FROM 1ST ADDR OF CHIPS A, B, C, & D
7	READ FROM 2ND ADDR OF CHIP A	READ FROM 2ND ADDR OF CHIPS A, B, C, & D
8	READ FROM 3RD ADDR OF CHIP A	READ FROM 3RD ADDR OF CHIPS A, B, C, & D
9	READ FROM 4TH ADDR OF CHIP A	READ FROM 4TH ADDR OF CHIPS A, B, C, & D
10	READ FROM 5TH ADDR OF CHIP A	READ FROM 5TH ADDR OF CHIPS A, B, C, & D
11	READ FROM 1ST ADDR OF CHIP B	READ FAIL FLAG FROM A
12	READ FROM 2ND ADDR OF CHIP B	READ FAIL FLAG FROM B
13	READ FROM 3RD ADDR OF CHIP B	READ FAIL FLAG FROM C
14	READ FROM 4TH ADDR OF CHIP B	READ FAIL FLAG FROM D
15	READ FROM 5TH ADDR OF CHIP B	
16	READ FROM 1ST ADDR OF CHIP C	
17	READ FROM 2ND ADDR OF CHIP C	
18	READ FROM 3RD ADDR OF CHIP C	
19	READ FROM 4TH ADDR OF CHIP C	
20	READ FROM 5TH ADDR OF CHIP C	
21	READ FROM 1ST ADDR OF CHIP D	
22	READ FROM 2ND ADDR OF CHIP D	
23	READ FROM 3RD ADDR OF CHIP D	
24	READ FROM 4TH ADDR OF CHIP D	
25	READ FROM 5TH ADDR OF CHIP D	

FIG. 4

	CLOCK CYCLE PRIOR ART TEST METHOD	CLOCK CYCLE EXEMPLARY TEST METHOD
1	WRITE TO 1ST ADDR OF CHIPS A, B, C, D, & E	WRITE TO 1ST ADDR OF CHIPS A, B, C, D, & E
2	WRITE TO 2ND ADDR OF CHIPS A, B, C, D, & E	WRITE TO 2ND ADDR OF CHIPS A, B, C, D, & E
3	WRITE TO 3RD ADDR OF CHIPS A, B, C, D, & E	WRITE TO 3RD ADDR OF CHIPS A, B, C, D, & E
4	WRITE TO 4TH ADDR OF CHIPS A, B, C, D, & E	WRITE TO 4TH ADDR OF CHIPS A, B, C, D, & E
5	READ FROM 1ST ADDR OF CHIP A	READ FROM 1ST ADDR OF CHIPS A, B, C, D, & E
6	READ FROM 2ND ADDR OF CHIP A	READ FROM 2ND ADDR OF CHIPS A, B, C, D, & E
7	READ FROM 3RD ADDR OF CHIP A	READ FROM 3RD ADDR OF CHIPS A, B, C, D, & E
8	READ FROM 4TH ADDR OF CHIP A	READ FROM 4TH ADDR OF CHIPS A, B, C, D, & E
9	READ FROM 1ST ADDR OF CHIP B	READ FAIL FLAG FROM A
10	READ FROM 2ND ADDR OF CHIP B	READ FAIL FLAG FROM B
11	READ FROM 3RD ADDR OF CHIP B	READ FAIL FLAG FROM C
12	READ FROM 4TH ADDR OF CHIP B	READ FAIL FLAG FROM D
13	READ FROM 1ST ADDR OF CHIP C	READ FAIL FLAG FROM E
14	READ FROM 2ND ADDR OF CHIP C	
15	READ FROM 3RD ADDR OF CHIP C	
16	READ FROM 4TH ADDR OF CHIP C	
17	READ FROM 1ST ADDR OF CHIP D	
18	READ FROM 2ND ADDR OF CHIP D	
19	READ FROM 3RD ADDR OF CHIP D	
20	READ FROM 4TH ADDR OF CHIP D	
21	READ FROM 1ST ADDR OF CHIP E	
22	READ FROM 2ND ADDR OF CHIP E	
23	READ FROM 3RD ADDR OF CHIP E	
24	READ FROM 4TH ADDR OF CHIP E	

FIG. 5

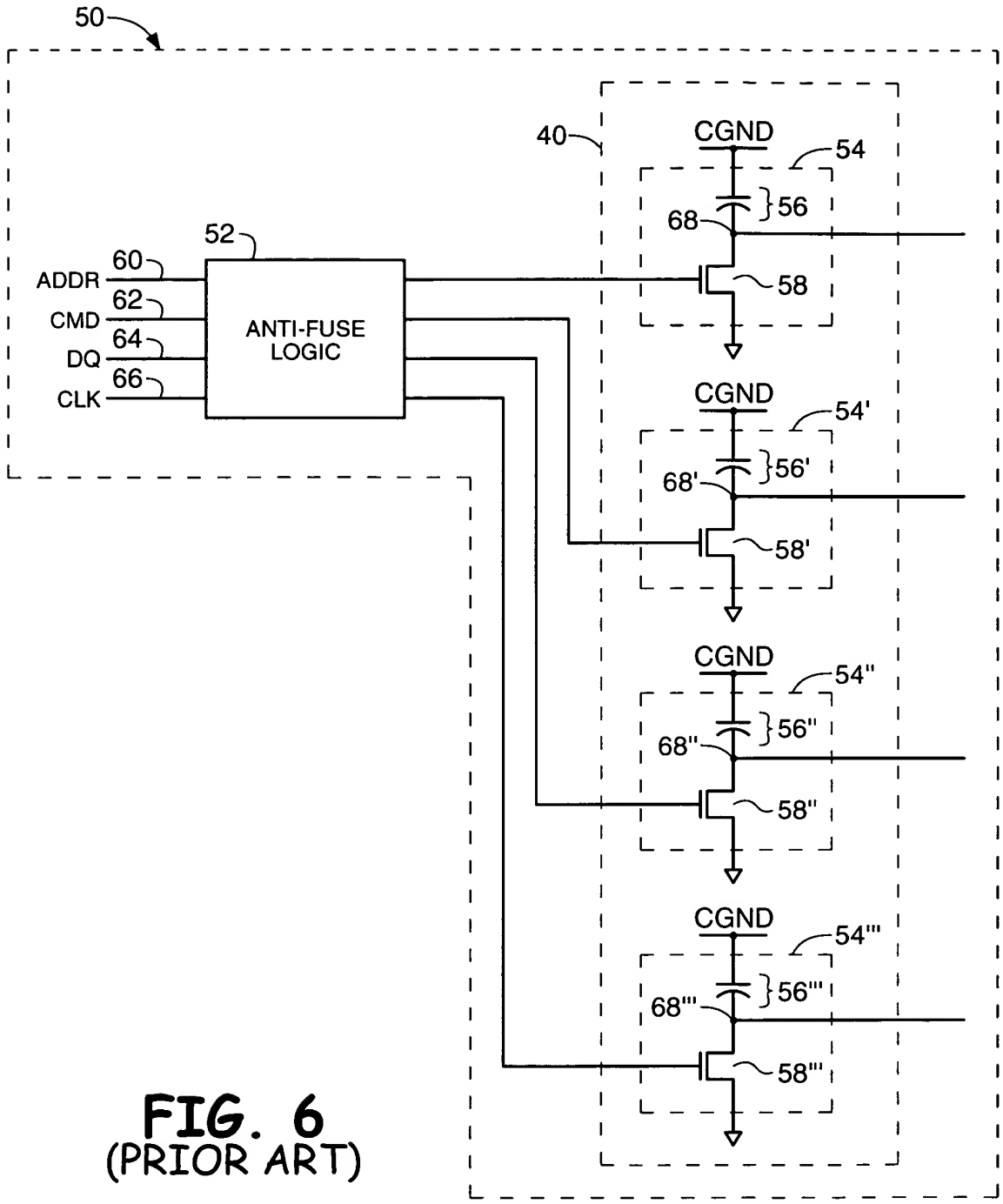

FIG. 6
(PRIOR ART)

	A	B	C	D
1ST ADDRESS	F	P	P	P
2ND ADDRESS	P	F	P	P
3RD ADDRESS	P	P	P	P
4TH ADDRESS	P	P	P	P

FIG. 7

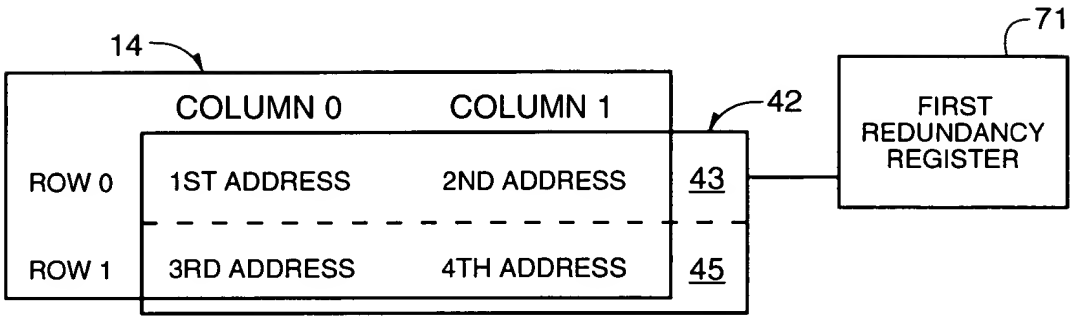

FIG. 9A

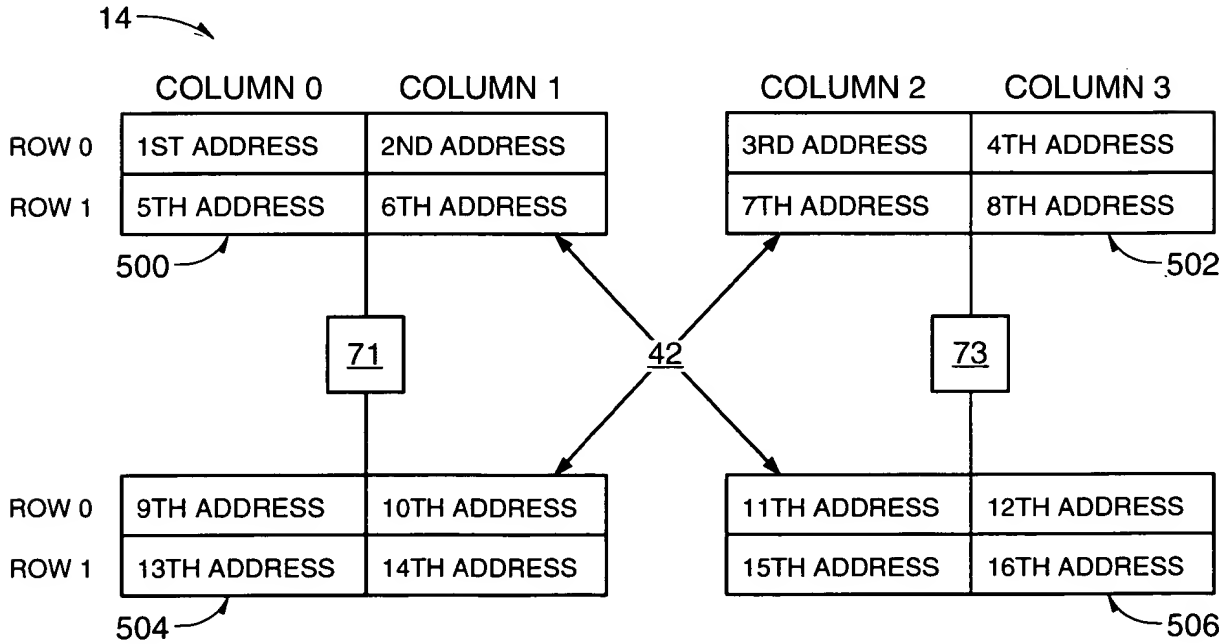

FIG. 9B

PRIOR ART REPAIR METHOD

ADDRESS	CMD	DQ
1ST ADDR TO A	BLOW 1ST FUSE	1
2ND ADDR TO A	BLOW 2ND FUSE	0
3RD ADDR TO A	BLOW 3RD FUSE	0
4TH ADDR TO A	BLOW 4TH FUSE	0
1ST ADDR TO B	BLOW 1ST FUSE	0
2ND ADDR TO B	BLOW 2ND FUSE	1
3RD ADDR TO B	BLOW 3RD FUSE	0
4TH ADDR TO B	BLOW 4TH FUSE	0
1ST ADDR TO C	BLOW 1ST FUSE	0
2ND ADDR TO C	BLOW 2ND FUSE	0
3RD ADDR TO C	BLOW 3RD FUSE	0
4TH ADDR TO C	BLOW 4TH FUSE	0
1ST ADDR TO D	BLOW 1ST FUSE	0
2ND ADDR TO D	BLOW 2ND FUSE	0
3RD ADDR TO D	BLOW 3RD FUSE	0
4TH ADDR TO D	BLOW 4TH FUSE	0

FIG. 8A
(PRIOR ART)

EXEMPLARY REPAIR METHOD

ADDRESS	CMD	DQ
COL 0 TO A-D	BLOW FUSE	DO NOT CARE
COL 1 TO A-D	BLOW FUSE	DO NOT CARE

FIG. 8B

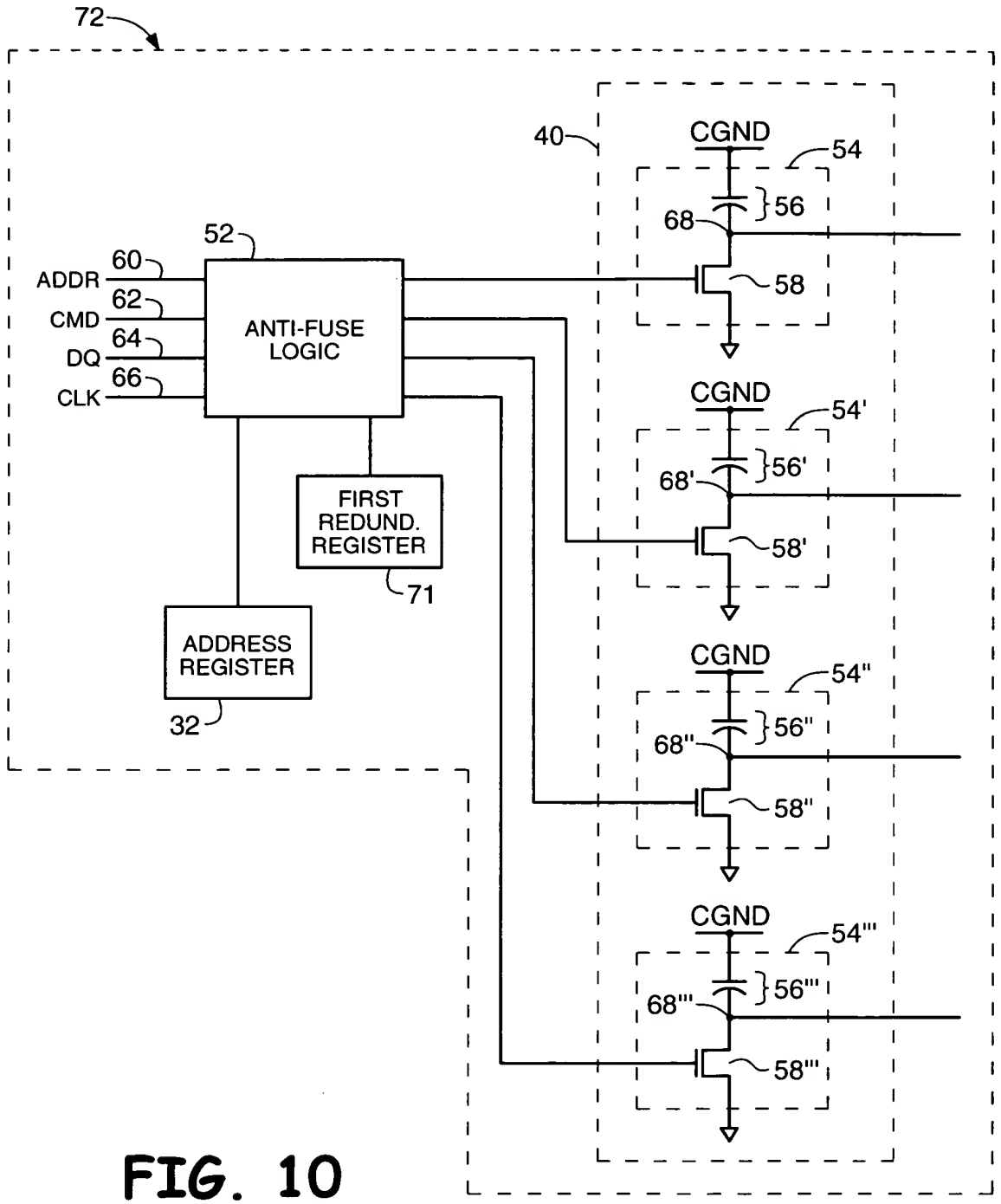
72
40
CGND
54
56
68
58
52
60
ADDR
62
CMD
64
DQ
66
CLK
ANTI-FUSE LOGIC
FIRST REDUND. REGISTER
71
ADDRESS REGISTER
32
54'
56'
68'
58'
54"
56"
68"
58"
54'''
56'''
68'''
58'''

FIG. 10

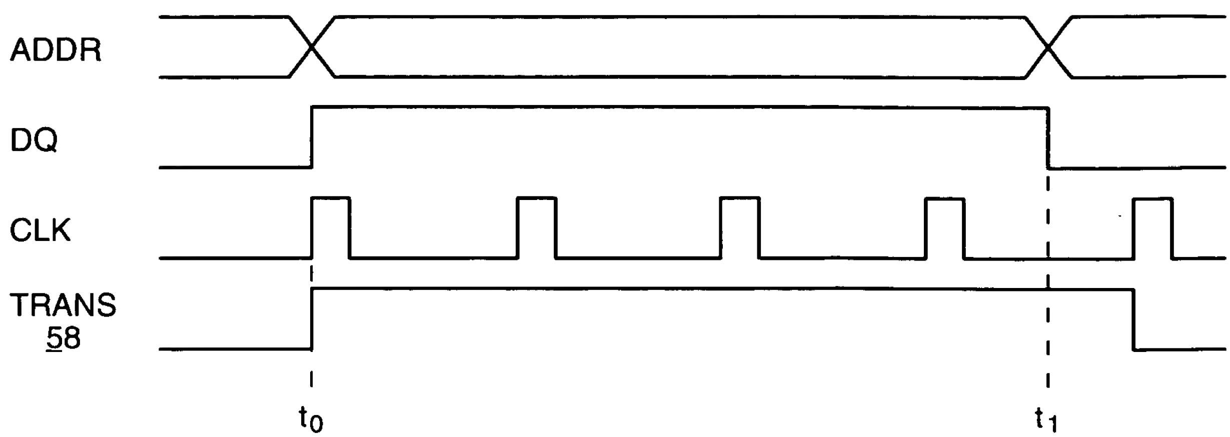

FIG. 11A (PRIOR ART)

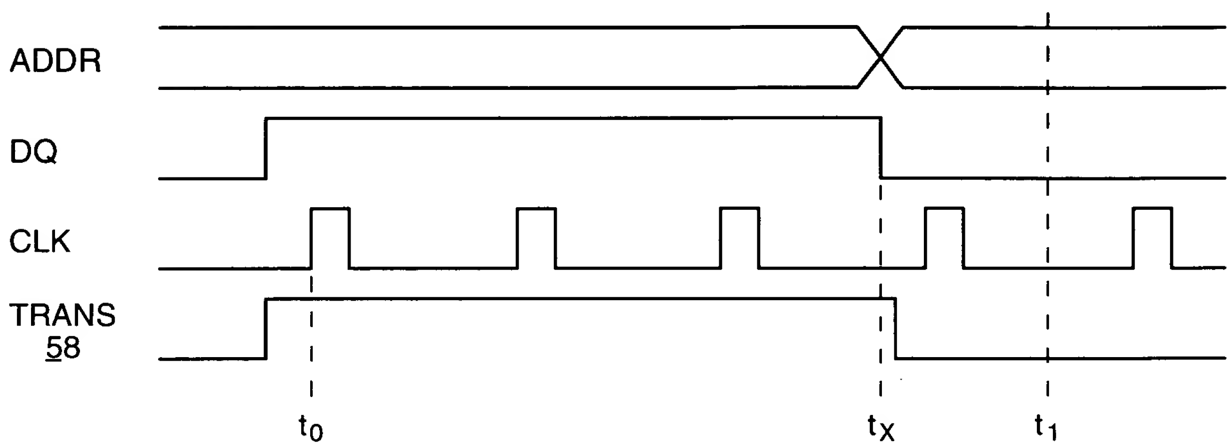

FIG. 11B (PRIOR ART)

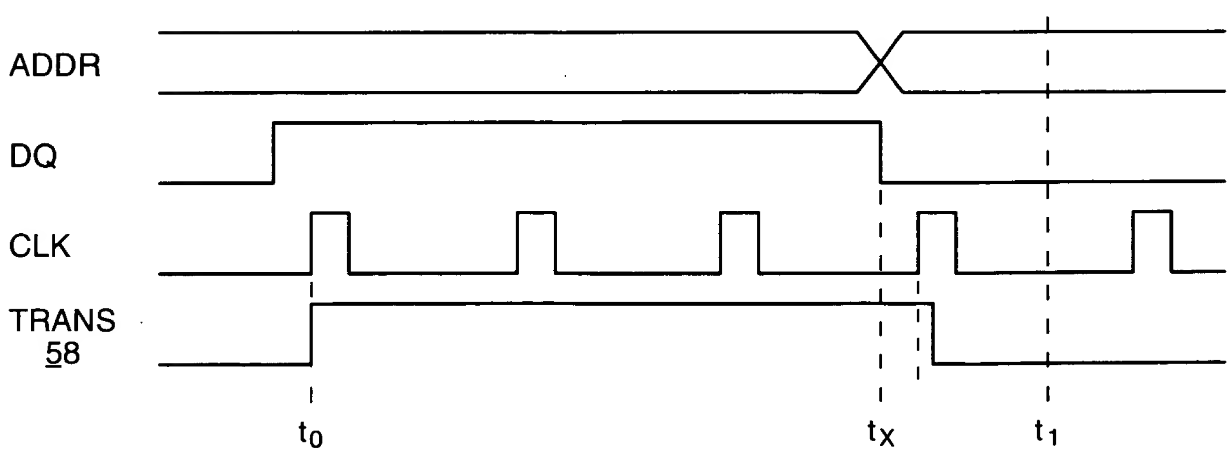

FIG. 11C (PRIOR ART)

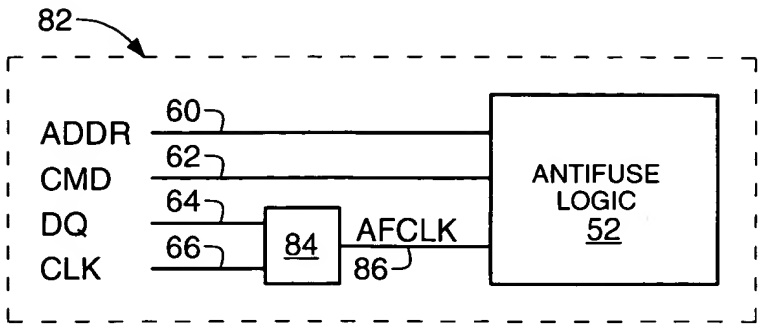

FIG. 12

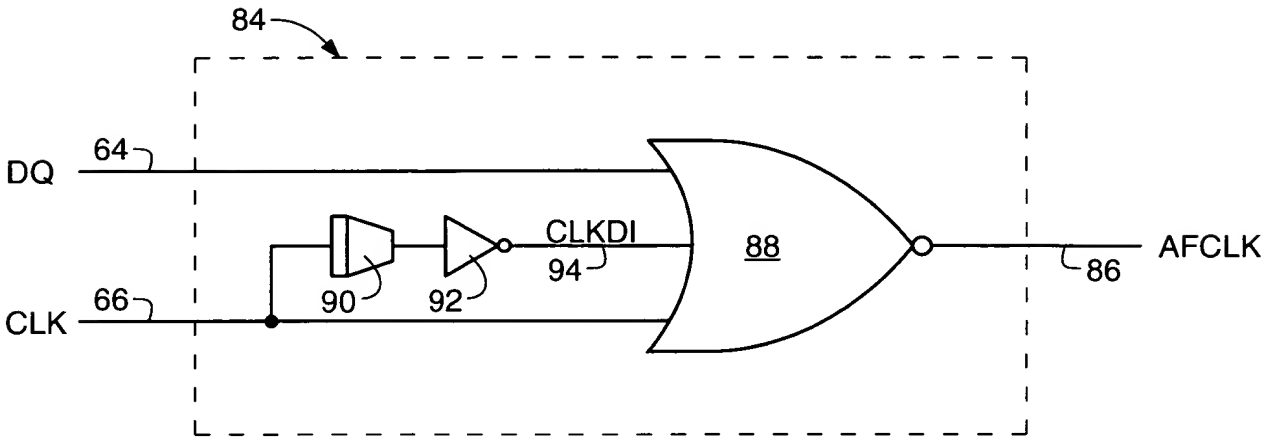

FIG. 13A

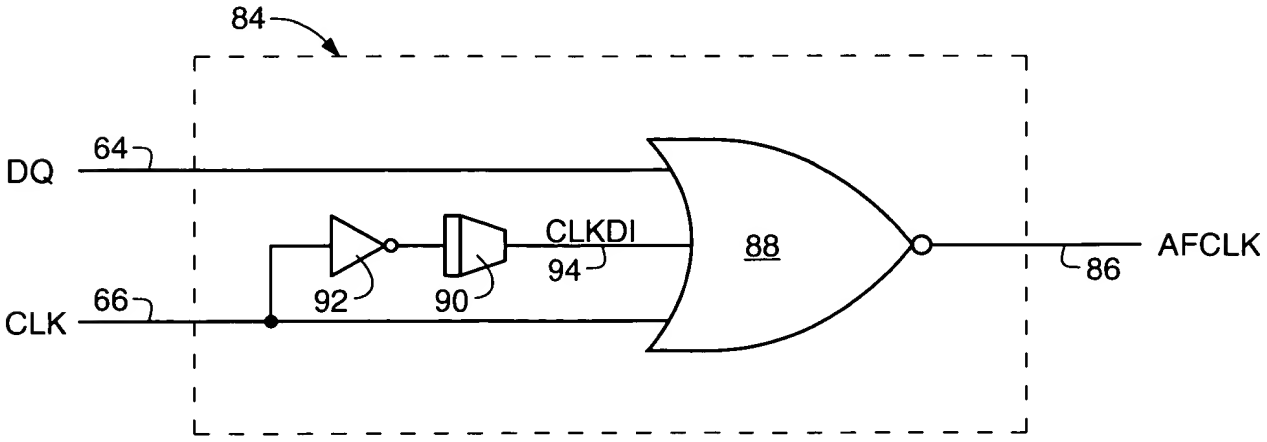

FIG. 13B

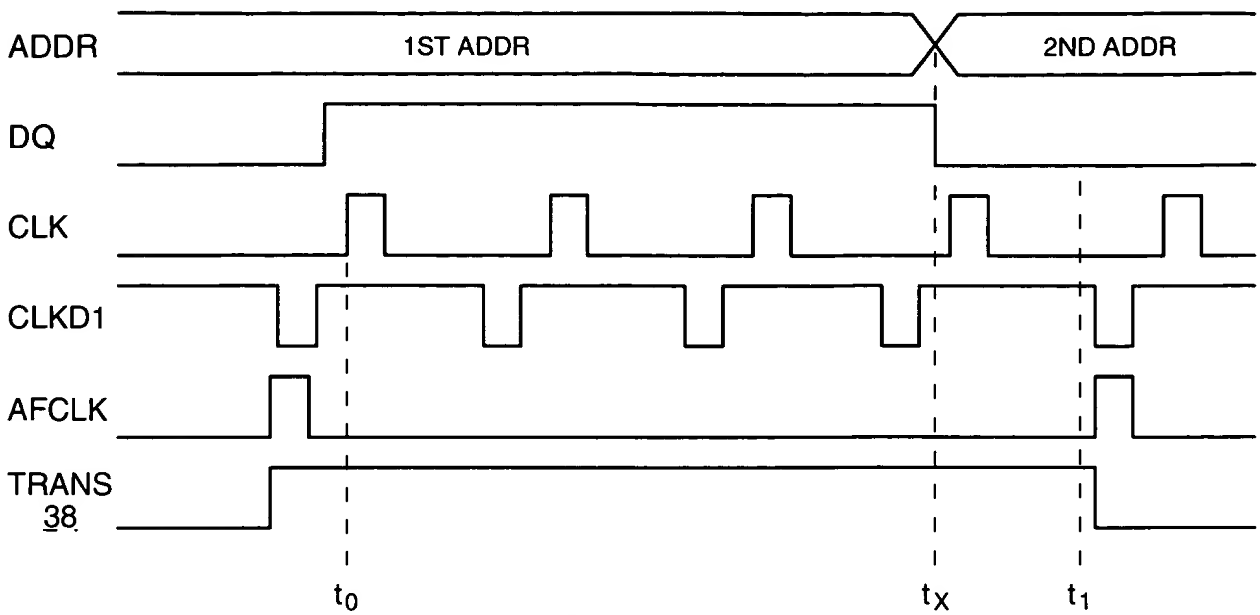
ADDR
1ST ADDR
2ND ADDR
DQ
CLK
CLKD1
AFCLK
TRANS
38
t_0
t_X
t_1

FIG. 14

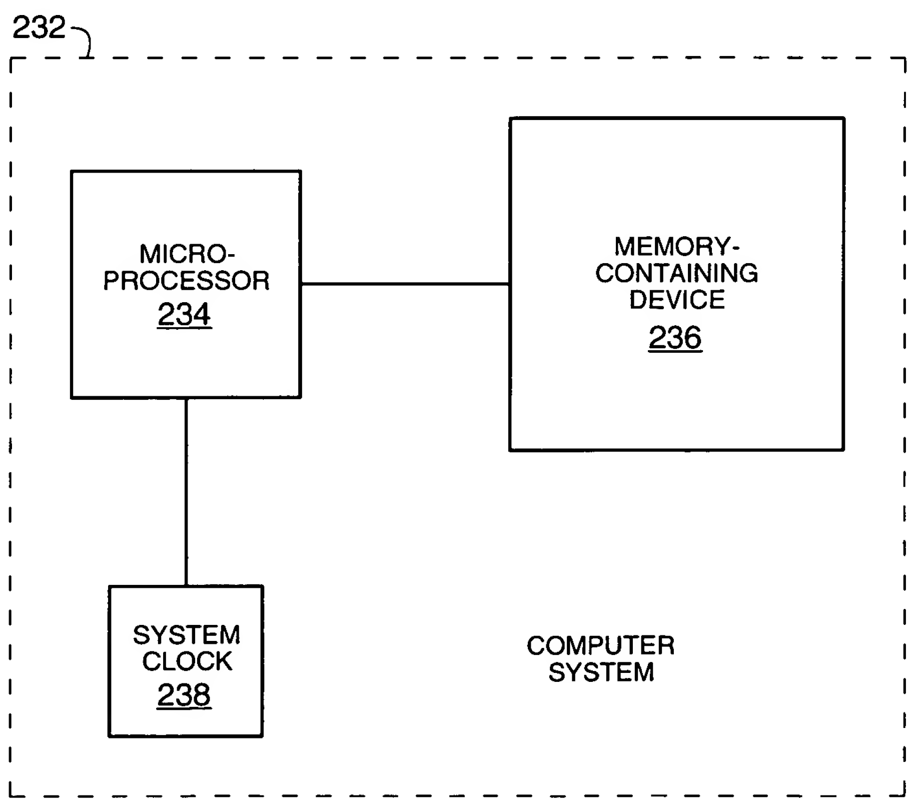
232
MICRO-
PROCESSOR
234
MEMORY-
CONTAINING
DEVICE
236
SYSTEM
CLOCK
238
COMPUTER
SYSTEM

FIG. 15